

**Claims**

We claim the following invention:

1. A System-on-Chip (SOC) interconnection apparatus, comprising:

a single semiconductor integrated circuit that includes one or more requestors and one or more addressable targets, wherein each said addressable target has a unique address space and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a sub-system;

an internal switching fabric that routes signals between said requestors and said addressable targets, said internal switching fabric further comprises one or more decoder/router elements, wherein each decoder/router element receives a request from a requestor, determines which said addressable target is the designated target using an internal system memory map, and routes said request to said designated target;

one or more requestor connection ports, wherein each said connection port connects one of said requestors to said internal switching fabric; and

one or more target connection ports, wherein each said target port connects one of said addressable targets to said internal switching fabric.

2. A system that includes a System-on-Chip (SOC) having an interconnection apparatus comprising:

a single semiconductor integrated circuit that includes one or more requestors and one or more addressable targets, wherein each said addressable target has a unique address space and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to

1 a device, an addressable bridge to a system, or an addressable bridge to a sub-system;  
2 an internal switching fabric that routes signals between said requestors and said  
3 addressable targets, said internal switching fabric further comprises one or more  
4 decoder/router elements, wherein each decoder/router element receives a request from  
5 a requestor, determines which said addressable target is the designated target using an  
6 internal system memory map, and routes said request to said designated target;

7 one or more requestor connection ports, wherein each said connection port  
8 connects one of said requestors to said internal switching fabric; and

9 one or more target connection ports, wherein each said target port connects one  
10 of said addressable targets to said internal switching fabric.

11 3. A method to make a System-on-Chip (SOC) interconnection apparatus,  
12 comprising:

13 providing a single semiconductor integrated circuit that includes one or more  
14 requestors and one or more addressable targets, wherein each said addressable target  
15 has a unique address space and further comprises one or more of the following:  
16 resident memory, a memory controller for resident or off-chip memory, an addressable  
17 bridge to a device, an addressable bridge to a system, or an addressable bridge to a  
18 subsystem;

19 coupling an internal switching fabric to said addressable targets and said  
20 requestors, said internal switching fabric routes signals between said requestors and  
21 said addressable targets, said internal switching fabric further comprises one or more  
22 decoder/router elements, wherein each decoder/router element receives a request from  
23 a requestor, determines which said addressable target is the designated target using an

1 internal system memory map, and routes said request to said designated target;  
2 providing one or more requestor connection ports, wherein each said connection  
3 port connects one of said requestors to said internal switching fabric; and  
4 providing one or more target connection ports, wherein each said target port  
5 connects one of said addressable targets to said internal switching fabric.

6 4. A method to use a System-on-Chip (SOC) interconnection apparatus,  
7 comprising:

8 receiving a request from one of one or more requestors over a requestor  
9 connection port coupled to said one requestor and to an internal switching fabric;

10 determining which one of one or more addressable targets is the designated  
11 target using an internal system memory map; and

12 routing said request to said designated target over a target connection port  
13 coupled to said internal switching fabric;

14 wherein said internal switching fabric, said one or more requestors, and said one  
15 or more addressable targets are all included on a single semiconductor integrated  
16 circuit, wherein each said addressable target has a unique address space and further  
17 comprises one or more of the following: resident memory, a memory controller for  
18 resident or off-chip memory, an addressable bridge to a device, an addressable bridge  
19 to a system, or an addressable bridge to a subsystem, and wherein said internal  
20 switching fabric routes signals between said requestors and said addressable targets  
21 and further comprises one or more decoder/router elements that receive said request  
22 from a requestor.

1 5. A program storage device readable by a computer that tangibly embodies a  
2 program of instructions executable by the computer to perform a method to use a  
3 System-on-Chip (SOC) interconnection apparatus, said method comprising:

4 receiving a request from one of one or more requestors over a requestor  
5 connection port coupled to said one requestor and to an internal switching fabric;

6 determining which one of one or more addressable targets is the designated  
7 target using an internal system memory map; and

8 routing said request to said designated target over a target connection port  
9 coupled to said internal switching fabric;

10 wherein said internal switching fabric, said one or more requestors, and said one  
11 or more addressable targets are all included on a single semiconductor integrated  
12 circuit, wherein each said addressable target has a unique address space and further  
13 comprises one or more of the following: resident memory, a memory controller for  
14 resident or off-chip memory, an addressable bridge to a device, an addressable bridge  
15 to a system, or an addressable bridge to a subsystem, and wherein said internal  
16 switching fabric routes signals between said requestors and said addressable targets  
17 and further comprises one or more decoder/router elements that receive said request  
18 from a requestor.

19 6. A dependent claim according to claim 1, 2, 3, 4, or 5, wherein said internal  
20 switching fabric further comprises one or more arbiters.

21 7. A dependent claim according to claim 1, 2, 3, 4, or 5, wherein one of said one or  
22 more decoder/router elements further comprises one of the following:

1 a decoder/router element that routes requests to all of said one or more  
2 addressable targets using an internal system memory map that includes unique  
3 address space information for all of said one or more addressable targets;

4 a decoder/router element that routes requests to less than all of said one or  
5 more addressable targets using an internal system memory map that includes unique  
6 address space information for all of said one or more addressable targets; or

7 a decoder/router element that routes requests to less than all of said one or  
8 more addressable targets using an internal system memory map that includes unique  
9 address space information for less than all of said one or more addressable targets.

10 8. A dependent claim according to claim 1, 2, 3, 4, or 5, wherein one of said one or  
11 more requestors and one of said one or more addressable targets together further  
12 comprise a single device having an independently accessible requestor port and an  
13 independently accessible target port.

14  
15 9. A dependent claim according to claim 1, 2, 3, 4, or 5, wherein one of said one or  
16 more addressable targets further comprises a single device having two independently  
17 accessible target ports.

18  
19 10. A dependent claim according to claim 1, 2, 3, 4, or 5, wherein said request  
20 routed to said designated target by said decoder/router element further comprises a  
21 registered, point-to-point signal that further comprises a plurality of pipeline stages.

1 11. A System-on-Chip (SOC) interconnection apparatus, comprising:  
2 a single semiconductor integrated circuit that includes one or more requestors  
3 and one or more addressable targets, wherein each said addressable target has a  
4 unique address space and further comprises one or more of the following: resident  
5 memory, a memory controller for resident or off-chip memory, an addressable bridge to  
6 a device, an addressable bridge to a system, or an addressable bridge to a subsystem;  
7 an internal switching fabric that routes signals between said requestors and said  
8 addressable targets, said internal switching fabric further comprises one or more  
9 decoder/router elements and one or more arbiters, wherein each decoder/router  
10 element receives a request from a requestor, determines which said addressable target  
11 is the designated target using an internal system memory map, and routes said request  
12 to said designated target, wherein said request routed to said designated target further  
13 comprises a registered, point-to-point signal having a plurality of pipeline stages;  
14 one or more requestor connection ports, wherein each said connection port  
15 connects one of said requestors to said internal switching fabric; and  
16 one or more target connection ports, wherein each said target port connects one  
17 of said addressable targets to said internal switching fabric;  
18 wherein one of said one or more decoder/router elements further comprises one  
19 of the following:  
20 a decoder/router element that routes requests to all of said one or more  
21 addressable targets using an internal system memory map that includes unique  
22 address space information for all of said one or more addressable targets;

1 a decoder/router element that routes requests to less than all of said one or  
2 more addressable targets using an internal system memory map that includes unique  
3 address space information for all of said one or more addressable targets; or

4 a decoder/router element that routes requests to less than all of said one or  
5 more addressable targets using an internal system memory map that includes unique  
6 address space information for less than all of said one or more addressable targets;  
7 and

8 wherein one of said one or more requestors and one of said one or more  
9 addressable targets together further comprise a single device having an independently  
10 accessible requestor port and an independently accessible target port; or

11 one of said one or more addressable targets further comprises a single device  
12 having two independently accessible target ports.

13  
14 12. A system that includes a System-on-Chip (SOC) having an interconnection  
15 apparatus comprising:

16 a single semiconductor integrated circuit that includes one or more requestors  
17 and one or more addressable targets, wherein each said addressable target has a  
18 unique address space and further comprises one or more of the following: resident  
19 memory, a memory controller for resident or off-chip memory, an addressable bridge to  
20 a device, an addressable bridge to a system, or an addressable bridge to a subsystem;

21 an internal switching fabric that routes signals between said requestors and said  
22 addressable targets, said internal switching fabric further comprises one or more

1 decoder/router elements and one or more arbiters, wherein each decoder/router  
2 element receives a request from a requestor, determines which said addressable target  
3 is the designated target using an internal system memory map, and routes said request  
4 to said designated target, wherein said request routed to said designated target further  
5 comprises a registered, point-to-point signal having a plurality of pipeline stages;

6 one or more requestor connection ports, wherein each said connection port  
7 connects one of said requestors to said internal switching fabric; and

8 one or more target connection ports, wherein each said target port connects one  
9 of said addressable targets to said internal switching fabric;

10 wherein one of said one or more decoder/router elements further comprises one  
11 of the following:

12 a decoder/router element that routes requests to all of said one or more  
13 addressable targets using an internal system memory map that includes unique  
14 address space information for all of said one or more addressable targets;

15 a decoder/router element that routes requests to less than all of said one or  
16 more addressable targets using an internal system memory map that includes unique  
17 address space information for all of said one or more addressable targets; or

18 a decoder/router element that routes requests to less than all of said one or  
19 more addressable targets using an internal system memory map that includes unique  
20 address space information for less than all of said one or more addressable targets;

21 and



1        wherein one of said one or more requestors and one of said one or more  
2        addressable targets together further comprise a single device having an independently  
3        accessible requestor port and an independently accessible target port; or

4        one of said one or more addressable targets further comprises a single device  
5        having two independently accessible target ports.

6        13.    A method to make a System-on-Chip (SOC) interconnection apparatus,  
7        comprising:

8               providing a single semiconductor integrated circuit that includes one or more  
9        requestors and one or more addressable targets, wherein each said addressable target  
10       has a unique address space and further comprises one or more of the following:  
11       resident memory, a memory controller for resident or off-chip memory, an addressable  
12       bridge to a device, an addressable bridge to a system, or an addressable bridge to a  
13       subsystem;

14              providing an internal switching fabric that routes signals between said requestors  
15       and said addressable targets, said internal switching fabric further comprises one or  
16       more decoder/router elements and one or more arbiters, wherein each decoder/router  
17       element receives a request from a requestor, determines which said addressable target  
18       is the designated target using an internal system memory map, and routes said request  
19       to said designated target, wherein said request routed to said designated target further  
20       comprises a registered, point-to-point signal having a plurality of pipeline stages;

21              providing one or more requestor connection ports, wherein each said connection  
22       port connects one of said requestors to said internal switching fabric; and

23              providing one or more target connection ports, wherein each said target port

1 connects one of said addressable targets to said internal switching fabric;

2 wherein one of said one or more decoder/router elements further comprises one  
3 of the following:

4 a decoder/router element that routes requests to all of said one or more  
5 addressable targets using an internal system memory map that includes unique  
6 address space information for all of said one or more addressable targets;

7 a decoder/router element that routes requests to less than all of said one or  
8 more addressable targets using an internal system memory map that includes unique  
9 address space information for all of said one or more addressable targets; or

10 a decoder/router element that routes requests to less than all of said one or  
11 more addressable targets using an internal system memory map that includes unique  
12 address space information for less than all of said one or more addressable targets;  
13 and

14 wherein one of said one or more requestors and one of said one or more  
15 addressable targets together further comprise a single device having an independently  
16 accessible requestor port and an independently accessible target port; or

17 one of said one or more addressable targets further comprises a single device  
18 having two independently accessible target ports.

19 14. A method to use a System-on-Chip (SOC) interconnection apparatus,  
20 comprising:

21 receiving a request from one of one or more requestors over a requestor

1 connection port coupled to said one requestor and to an internal switching fabric;  
2 determining which one of one or more addressable targets is the designated  
3 target using an internal system memory map; and  
4 routing said request to said designated target over a target connection port  
5 coupled to said internal switching fabric, wherein said request routed to said designated  
6 target further comprises a registered, point-to-point signal having a plurality of pipeline  
7 stages;  
8 wherein said internal switching fabric, said one or more requestors, and said one  
9 or more addressable targets are all included on a single semiconductor integrated  
10 circuit, wherein each said addressable target has a unique address space and further  
11 comprises one or more of the following: resident memory, a memory controller for  
12 resident or off-chip memory, an addressable bridge to a device, an addressable bridge  
13 to a system, or an addressable bridge to a subsystem, and wherein said internal  
14 switching fabric routes signals between said requestors and said addressable targets  
15 and further comprises one or more arbiters and one or more decoder/router elements  
16 that receive said request from a requestor;  
17 wherein one of said one or more decoder/router elements further comprises one  
18 of the following:  
19 a decoder/router element that routes requests to all of said one or more  
20 addressable targets using an internal system memory map that includes unique  
21 address space information for all of said one or more addressable targets;

1 a decoder/router element that routes requests to less than all of said one or  
2 more addressable targets using an internal system memory map that includes unique  
3 address space information for all of said one or more addressable targets; or

4 a decoder/router element that routes requests to less than all of said one or  
5 more addressable targets using an internal system memory map that includes unique  
6 address space information for less than all of said one or more addressable targets;  
7 and

8 wherein one of said one or more requestors and one of said one or more  
9 addressable targets together further comprise a single device having an independently  
10 accessible requester port and an independently accessible target port; or

11 one of said one or more addressable targets further comprises a single device  
12 having two independently accessible target ports.

13  
14 15. A program storage device readable by a computer that tangibly embodies a  
15 program of instructions executable by the computer to perform a method to use a  
16 System-on-Chip (SOC) interconnection apparatus, said method comprising:

17 receiving a request from one of one or more requestors over a requestor  
18 connection port coupled to said one requestor and to an internal switching fabric;

19 determining which one of one or more addressable targets is the designated  
20 target using an internal system memory map; and

21 routing said request to said designated target over a target connection port  
22 coupled to said internal switching fabric, wherein said request routed to said designated

1 target further comprises a registered, point-to-point signal having a plurality of pipeline  
2 stages;

3 wherein said internal switching fabric, said one or more requestors, and said one  
4 or more addressable targets are all included on a single semiconductor integrated  
5 circuit, wherein each said addressable target has a unique address space and further  
6 comprises one or more of the following: resident memory, a memory controller for  
7 resident or off-chip memory, an addressable bridge to a device, an addressable bridge  
8 to a system, or an addressable bridge to a subsystem, and wherein said internal  
9 switching fabric routes signals between said requestors and said addressable targets  
10 and further comprises one or more memory arbiters and one or more decoder/router  
11 elements that receive said request from a requestor;

12 wherein one of said one or more decoder/router elements further comprises one  
13 of the following:

14 a decoder/router element that routes requests to all of said one or more  
15 addressable targets using an internal system memory map that includes unique  
16 address space information for all of said one or more addressable targets;

17 a decoder/router element that routes requests to less than all of said one or  
18 more addressable targets using an internal system memory map that includes unique  
19 address space information for all of said one or more addressable targets; or

20 a decoder/router element that routes requests to less than all of said one or  
21 more addressable targets using an internal system memory map that includes unique

1 address space information for less than all of said one or more addressable targets;  
2 and

3 wherein one of said one or more requestors and one of said one or more  
4 addressable targets together further comprise a single device having an independently  
5 accessible requestor port and an independently accessible target port; or

6 one of said one or more addressable targets further comprises a single device  
7 having two independently accessible target ports.